WHAT IS CLAIMED IS:

1. A fuse circuit comprising blocks, wherein each of the blocks comprises a sub-fuse set constituted of fuse elements electrically programmable,

5   and a program control circuit which controls programming of the fuse elements,

one of the fuse elements is an enable bit representing validity/invalidity of the sub-fuse set, and

10   the program control circuit determines a block becoming an object of the programming among the blocks in accordance with a value of the enable bit.

2. The fuse circuit according to claim 1, further comprising a program data latch circuit which latches

15   program data for the block becoming the object of the programming.

3. The fuse circuit according to claim 1, wherein the blocks are series connected in n stages (n = plural number), and

20   in the block in a first stage, the program control circuit determines whether or not the block in the first block becomes the object of the programming in accordance with the value of the enable bit in the first block.

25   4. The fuse circuit according to claim 3, wherein when the value of the enable bit in the first block represents the invalidity of the sub-fuse set,

the block in the first stage becomes the object of
the programming.

5. The fuse circuit according to claim 1, wherein
the blocks are series connected in n stages
(n = plural number), and

in the block in an i-th stage (2 ≤ i ≤ n), the
program control circuit determines whether or not the
block in the i-th stage becomes the object of the
programming in accordance with a value of the enable
bit in the block in an (i-1)th stage and a value of the
enable bit in the block in the i-th stage.

6. The fuse circuit according to claim 5, wherein
when the value of the enable bit in the block in the
(i-1)th stage represents the validity of the sub-fuse
set and when the value of the enable bit in the block
in the i-th block represents the invalidity of the
sub-fuse set, the block in the i-th stage becomes the
object of the programming.

7. The fuse circuit according to claim 1, wherein
each of the blocks has a read control circuit
which controls a read of fuse data programmed into each
of the fuse elements, and

the read control circuit determines a block
becoming an object of the read among the blocks in
accordance with a value of the enable bit.

8. The fuse circuit according to claim 7, wherein
the blocks are series connected in n stages

(n = plural number), and

in the block in an i-th stage (1 ≤ i ≤ n-1), the read control circuit determines whether or not the block in the i-th stage becomes the object of the read in accordance with a value of the enable bit in the block in the i-th stage and a value of the enable bit in the block in an (i+1)th stage.

9. The fuse circuit according to claim 8, wherein when the value of the enable bit in the block in the i-th block represents the validity of the sub-fuse set and when the value of the enable bit in the block in (i+1)th stage represents the invalidity of the sub-fuse set, the block in the i-th stage becomes the object of the read.

10. The fuse circuit according to claim 7, wherein the blocks are series connected in n stages (n = plural number), and

in the block in an n-th stage, the read control circuit determines whether or not the block in the n-th stage becomes the object of the read in accordance with a value of the enable bit in the block in the n-th stage.

11. The fuse circuit according to claim 10, wherein when the value of the enable bit in the block in the n-th block represents the validity of the sub-fuse set, the block in the n-th stage is becomes the object of the read.

12.   The fuse circuit according to claim 1, wherein each of the blocks has a read data latch circuit which latches fuse data read from the fuse elements.

13.   The fuse circuit according to claim 1, wherein each of the blocks has a read data latch circuit which latches the enable bit read from one of the fuse elements, and

read data latch circuits which latch the remaining fuse data excluding the enable bit are shared by the blocks.

14.   The fuse set according to claim 1, wherein each of the fuse elements is an electric fuse element or an anti-fuse element.

15.   The fuse element according to claim 1, wherein the blocks are series connected in n stages (n = plural number), and

the block becoming the object of the programming is determined in the direction from the block in the first block to the block in the n-th block in units of a data rewrite.

16.   An integrated circuit having at least one function block comprising a memory which non-volatilely stores data regarding the integrated circuit, wherein the memory is the fuse circuit according to claim 1, and

the data regarding the integrated circuit is rewritable.

17.   A read/program method comprising performing programming for a fuse circuit having sub-fuse sets series connected in n stages, the method comprising:

automatically sequentially changing a sub-fuse set becoming an object of the programming in the direction from the sub-fuse set in the first stage to the sub-fuse set in the n-th stage; and

executing a data rewrite into the object of the programming for the fuse circuit.

18.   The read/program method according to claim 17, wherein the sub-fuse set becoming the object of the programming is automatically determined immediately after power on in accordance with a value of an enable bit representing validity/invalidity of the sub-fuse set.

19.   The read/program method according to claim 18, wherein the sub-fuse set becoming an object of a fuse-data read is automatically determined immediately after power on in accordance with the value of the enable bit, or , after power on, the enable bit is first latched into a read data latch circuit, and the fuse data in the sub-fuse set is then latched into a read data latch circuit after the sub-fuse set becoming the object of the fuse-data read has been determined.